

3N209-3N210

DUAL GATE MOSFET VHF AMPLIFIER

High-reliability discrete products and engineering services since 1977

FEATURES

- Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.
- Available as non-RoHS (Sn/Pb plating), standard, and as RoHS by adding "-PBF" suffix.

MAXIMUM RATINGS

Rating	Symbol	Va	lue	Unit
Drain – source voltage	V _{DS}	25		Vdc
Drain gate voltage	V _{DG1} V _{DG2}	30		Vdc
Gate current	I _{G1R} I _{G1F} I _{G2R}	-10 10 -10		mAdc
	I _{G2F}	10		
Drain current – continuous	I _D	30		mAdc
Total power dissipation @ $T_A = 25^{\circ}C$		3N209	3N210	
Derate above 25°C	P _D	300 1.71	350 2.80	mW mW/°C
Storage channel temperature range	T _{stg}	-65 to 200	-65 to 175	°C
Operating channel temperature	T _{channel}	200	150	°C
Lead temperature, 1/16" from seated surface for 10 s		260		°C

ELECTRICAL CHARACTERISTICS (T_c = 25°C)

Characteristic	Symbol	Min	Тур	Max	Unit
OFF CHARACTERISTICS					
Drain source breakdown voltage	N				Vda
$(I_D = 10 \mu Adc, V_{G1S} = -4.0 Vdc, V_{G2S} = 4.0 Vdc)$	V _{(BR)DS}	25	-	-	Vdc
Gate 1 – source forward breakdown voltage	V				Vdc
$(I_{G1} = 10 \text{ mAdc}, V_{G2S} = V_{DS} = 0)$	V _{(BR)G1SSF}	7.0	-	22	vuc
Gate 1 – source reverse breakdown voltage					Vdc
$(I_{G1} = -10 \text{mAdc}, V_{G2S} = V_{DS} = 0)$	V _{(BR)G1SSR}	7.0	-	-22	vuc
Gate 2 – source forward breakdown voltage					Vdc
$(I_{G2} = 10 \text{ mAdc}, V_{G1S} = V_{DS} = 0)$	V _{(BR)G2SSF}	7.0	-	22	vuc
Gate 2 – source reverse breakdown voltage	V				Vdc
$(I_{G2} = -10 \text{mAdc}, V_{G1S} = V_{DS} = 0)$	V _{(BR)G2SSR}	-7.0	-	-22	
Gate 1 – source cutoff voltage				Vdc	
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} = 50\mu Adc)$	V _{G1S(off)}	-0.1	-	-4.0	vuc
Gate 2 – source cutoff voltage	N/				Vdc
$(V_{DS} = 15Vdc, V_{G1S} = 0Vdc, I_{D} = 50\mu Adc)$	V _{G2S(off)}	-0.1	-	-4.0	vuc
Gate 1 – terminal forward current				nAdc	
$(V_{G1S} = 6.0Vdc, V_{G2S} = V_{DS} = 0)$	IGISSF	-	-	20	nauc
Gate 1 – terminal reverse current					
$(V_{G1S} = -6.0Vdc, V_{G2S} = V_{DS} = 0)$	I _{G1SSR}	-	-	-20	nAdc
$(V_{G1S} = -6.0Vdc, V_{G2S} = V_{DS} = 0, T_A = 150^{\circ}C)$		-	-	-10	μAdc



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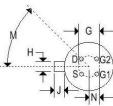
Characteristic	Symbol	Min	Тур	Max	Unit	
Gate 2 – terminal forward current						
$(V_{G2S} = 6.0Vdc, V_{G1S} = V_{DS} = 0)$	I _{G2SSF}	-	-	20	nAdc	
Gate 2 – terminal reverse current						
$(V_{G2S} = -6.0Vdc, V_{G1S} = V_{DS} = 0)$	I _{G2SSR}	-	-	-20	nAdc	
$(V_{G2S} = -6.0vdc, V_{G1S} = V_{DS} = 0, T_A = 150^{\circ}C)$		-	-	-10	μAdc	
ON CHARACTERISTICS						
Gate 1 – zero voltage drain current		5.0	-	30	mAdc	
$(V_{DS} = 15Vdc, V_{G1S} = 0, V_{G2S} = 4.0Vdc)$	I _{DSS}					
SMALL SIGNAL CHARACTERISTICS						
Forward transfer admittance					Ι.	
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} = 10mAdc, f = 1.0kHz)$	Υfs	10	13	20	mmhos	
Input capacitance	6				- 5	
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} \ge 5.0mAdc, f = 1.0MHz)$	C _{iss}	-	4.5	7.0	pF	
Reverse transfer capacitance	C _{rss}				~ Г	
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} \ge 5.0mAdc, f = 1.0MHz)$	Crss	0.005	0.023	0.030	pF	
Dutput capacitance			- 5			
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} \ge 5.0mAdc, f = 1.0MHz)$	C _{oss}	0.5	2.0	4.0	pF	
Common source noise figure	NF				dB	
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_{D} \ge 10mAdc, f = 500MHz)$	NF	-	4.5	6.0	aв	
Common source power gain		10				
$(V_{DS} = 15Vdc, V_{G2S} = 4.0Vdc, I_D \ge 10mAdc, f = 500MHz)$	G _{ps}	10	13	20	dB	
Bandwidth			MHz			
(V _{DS} = 15Vdc, V _{G2S} = 4.0Vdc; I _D = 10mAdc, f = 500MHz)	BW	7.0	-	17	171112	

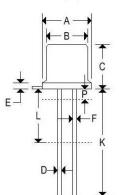


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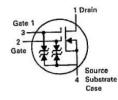
MECHANICAL CHARACTERISTICS

Case:	TO-72
Marking:	Body painted, alpha-numeric
Pin out:	See below





	TO-72				
	Inches		Millim	eters	
	Min	Max	Min	Max	
Α		0.230		5.840	
В	(2)	0.195	(74)	4.950	
С		0.210	9	5.330	
D	(4)	0.021	188 L	0.530	
E	-	0.030		0.760	
F		0.019	-	0.480	
G	0.100 BSC		2.540	BSC	
Н	-	0.046	-	1.170	
J	-	0.048		1.220	
К	0.500		12.700	1	
L	0.250		200	6.350	
М	45° BSC		45° BSC		
Ν	0.050 BDC		1.270 BSC		
Р	12	0.050	74)	1.270	



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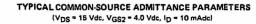
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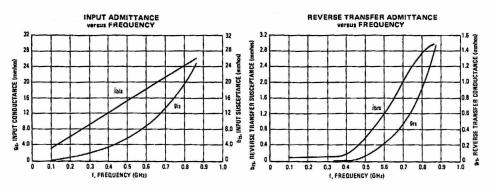


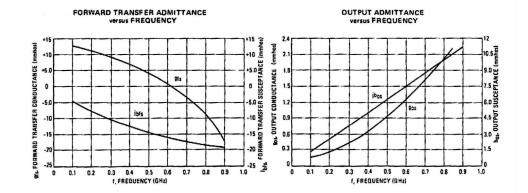
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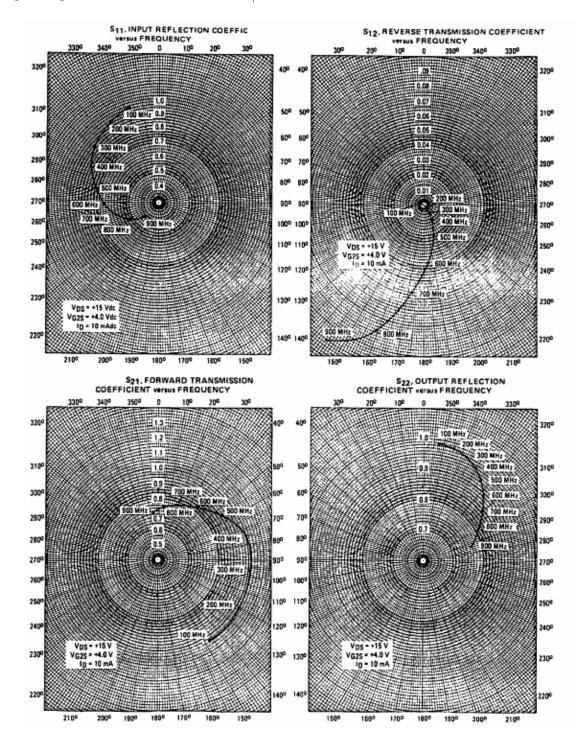




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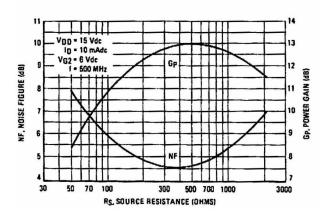


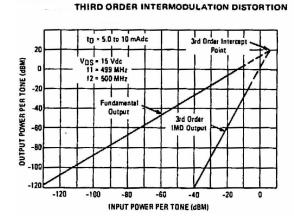
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POWER GAIN AND NOISE FIGURE Versus SOURCE RESISTANCE





TEST CIRCUIT FOR POWER GAIN, NOISE FIGURE AND THIRD ORDER INTERMODULATION DISTORTION

