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High-reliability discrete products
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MJ13333

NPN SILICON POWER TRANSISTOR

FEATURES

- Available as "HR" (high reliability) screened per MIL-PRF-19500, JANTX level. Add "HR" suffix to base part number.
- Available as non-RoHS (Sn/Pb plating), standard, and as RoHS by adding "-PBF" suffix.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Collector emitter voltage	V_{CEO}	400	Vdc
Collector emitter voltage	V_{CEV}	700	Vdc
Emitter base voltage	V_{EB}	6.0	Vdc
Collector current **-Continuous** **-Peak** (1)	 I_C I_{CM}	 20 30	Adc
Base current **-Continuous** **-Peak** (1)	 I_B I_{BM}	 10 15	Adc
Total power dissipation @ T_C = 25°C **Total power dissipation @ T_C = 100°C** **Derate above 25°C**	P_D	175 100 1	W W W/°C
Operating and storage temperature range	T_J, T_{stg}	-65 to +200	°C
Thermal resistance, junction to case	$R_{\Theta JC}$	1.0	°C/W
Maximum lead temperature for soldering purposes: **1/8" from case for 5 seconds**	T_L	275	°C

Note 1: Pulse test: pulse width = 5ms, duty cycle ≤ 10%.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Collector emitter sustaining voltage (I_C = 100mA, I_B = 0)	$V_{CEO(sus)}$	400	-	-	Vdc
Collector cutoff current (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5Vdc) (V_{CEV} = Rated Value, $V_{BE(off)}$ = 1.5Vdc, T_C = 150°C)	I_{CEV}	- -	- -	0.25 5	mAdc
Collector cutoff current (V_{CE} = Rated V_{CEV}, R_{BE} = 50Ω, T_C = 100°C)	I_{CER}	-	-	5	mAdc
Emitter cutoff current (V_{EB} = 6Vdc, I_C = 0)	I_{EBO}	-	-	1.0	mAdc
SECOND BREAKDOWN					
Second breakdown collector current with base forward biased	$I_{S/b}$	Figure 12			
Clamped inductive SOA with base reverse biased	RBSOA	Figure 13			
ON CHARACTERISTICS (2)					
DC current gain (I_C = 5Adc, V_{CE} = 5Vdc)	h_{FE}	10	-	60	-

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ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified)

Characteristic		Symbol	Min	Typ	Max	Unit
Collector emitter saturation voltage						
(I_C = 10Adc, I_B = 2.0Adc)		$V_{CE(sat)}$	-	-	1.8	Vdc
(I_C = 20Adc, I_B = 6.7Adc)			-	-	5.0	
(I_C = 10Adc, I_B = 2.0Adc, T_C = 100°C)			-	-	2.4	
Base-emitter saturation voltage						
(I_C = 10Adc, I_B = 2.0Adc)		$V_{BE(sat)}$	-	-	1.8	Vdc
(I_C = 10Adc, I_B = 2.0Adc, T_C = 100°C)			-	-	1.8	
DYNAMIC CHARACTERISTICS						
Output capacitance (V_{CB} = 10Vdc, I_E = 0, f_{test} = 1.0kHz)		C_{ob}	125	-	500	pF
SWITCHING CHARACTERISTICS						
Resistive load						
Delay time	(V_{CC} = 250Vdc, I_C = 10A, I_{B1} = 2.0A, $V_{BE(off)}$ = 5Vdc, t_p = 10µs, duty cycle ≤ 2%)	t_d	-	0.02	0.1	µs
Rise time		t_r	-	0.3	0.7	
Storage time		t_s	-	1.6	4.0	
Fall time		t_f	-	0.3	0.7	
Inductive load (clamped)						
Storage time	(I_C = 10A(pk), V_{clamp} = 250Vdc, I_{B1} = 2.0A, $V_{BE(off)}$ = 5Vdc, T_C = 100°C)	t_{sv}	-	2.5	5.0	µs
Crossover time		t_c	-	0.8	2.0	
Storage time	(I_C = 10A(pk), V_{clamp} = 250Vdc, I_{B1} = 2.0A, $V_{BE(off)}$ = 5Vdc, T_C = 25°C)	t_{sv}	-	1.8	-	µs
Crossover time		t_c	-	0.4	-	
Fall time		t_f	-	0.2	-	

Note 2: Pulse test: pulse width = 300µs, duty cycle ≤ 2%.

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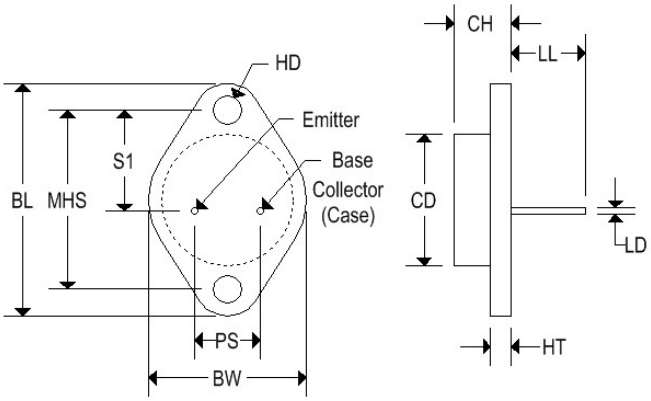
MECHANICAL CHARACTERISTICS

Case	TO-3
Marking	Alpha-numeric
Polarity	See below



	TO-3			
	Inches		Millimeters	
	Min	Max	Min	Max
CD	-	0.875	-	22.220
CH	0.250	0.380	6.860	9.650
HT	0.060	0.135	1.520	3.430
BW	-	1.050	-	26.670
HD	0.131	0.188	3.330	4.780
LD	0.038	0.043	0.970	1.090
LL	0.312	0.500	7.920	12.700
BL	1.550 REF		39.370 REF	
MHS	1.177	1.197	29.900	30.400
PS	0.420	0.440	10.670	11.180
S1	0.655	0.675	16.640	17.150

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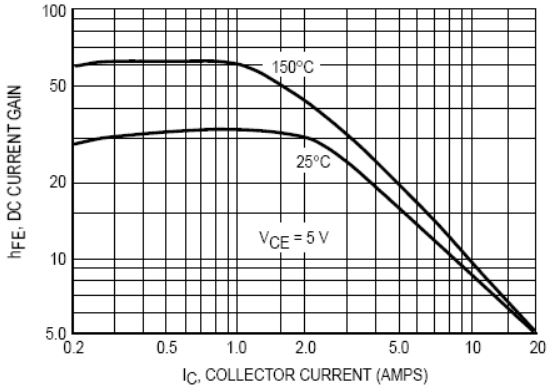

Figure 1. DC Current Gain

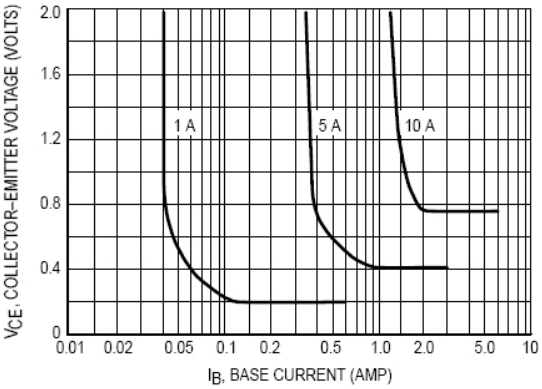

Figure 2. Collector Saturation Region

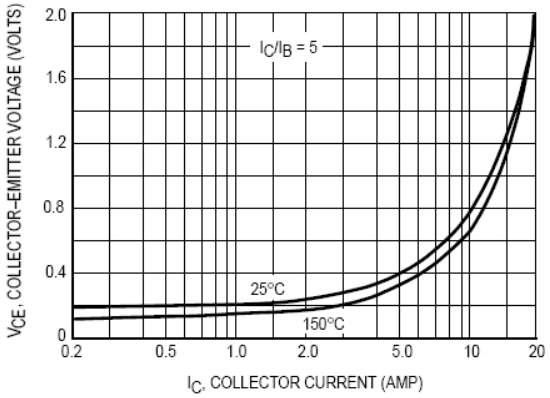

Figure 3. Collector–Emitter Saturation Region

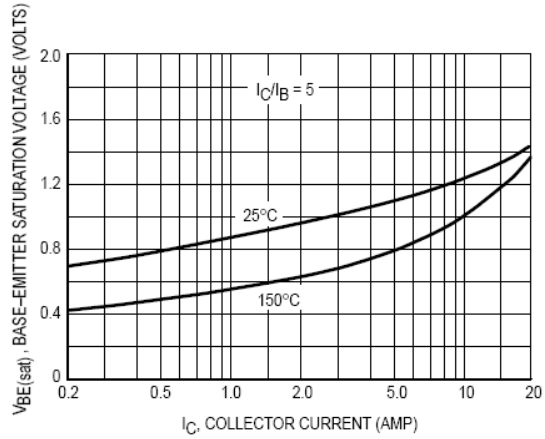

Figure 4. Base–Emitter Voltage

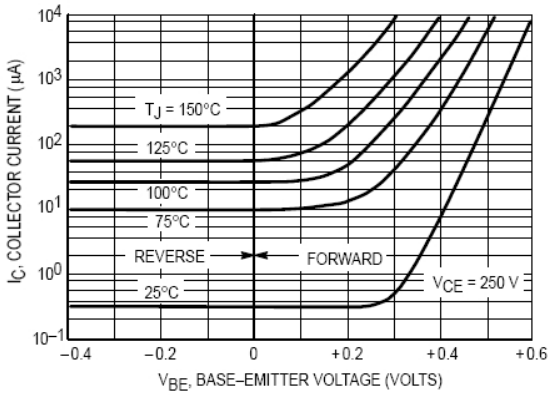

Figure 5. Collector Cutoff Region

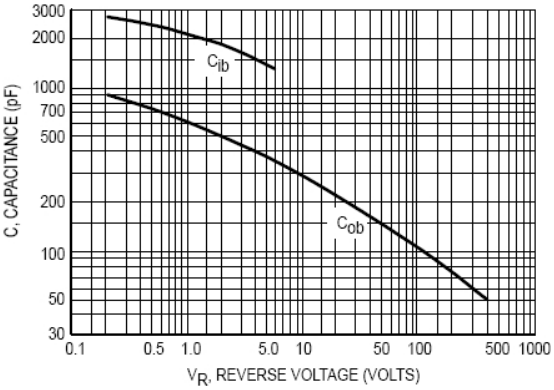

Figure 6. Capacitance

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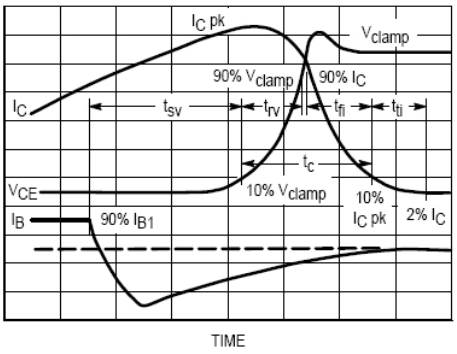

Figure 7. Inductive Switching Measurements

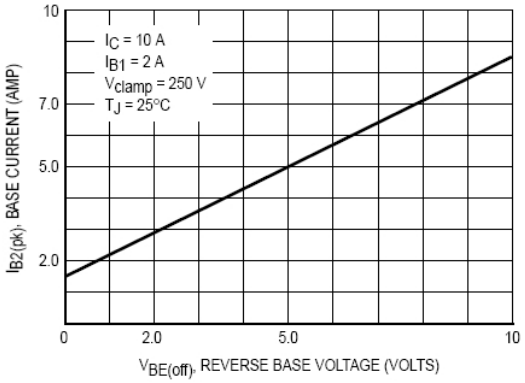

Figure 8. Reverse Base Current versus $V_{BE(off)}$ With No External Base Resistance

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

t_{sv} = Voltage Storage Time, 90% I_{B1} to 10% V_{clamp}
t_{rv} = Voltage Rise Time, 10 – 90% V_{clamp}
t_{fi} = Current Fall Time, 90 – 10% I_C
t_{ti} = Current Tail, 10 – 2% I_C
t_c = Crossover Time, 10% V_{clamp} to 10% I_C

An enlarged portion of the inductive switching waveforms is shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN–222:

$$P_{SWT} = 1/2\ V_{CC} I_C (t_c) f$$

In general, $t_{rv} + t_{fi} \simeq t_c$. However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers, However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds (t_c and t_{sv}) which are guaranteed at 100°C.

RESISTIVE SWITCHING PERFORMANCE

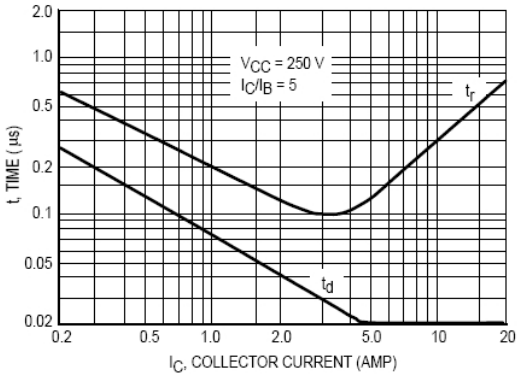

Figure 9. Turn–On Switching Times

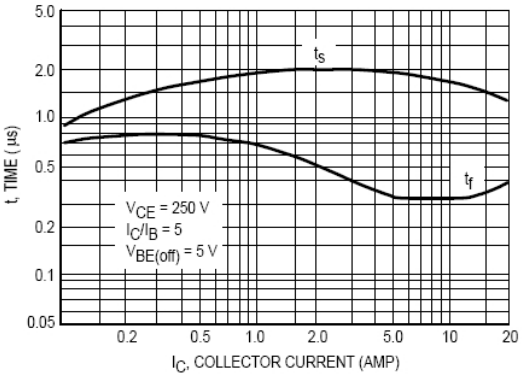

Figure 10. Turn–Off Switching Times

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Table 1. Test Conditions for Dynamic Performance

	$V_{CEO(sus)}$	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	+10 V, 20, 1, 0, 2 PW Varied to Attain I_C = 100 mA	250 µF, 470 Ω 2 W, 47 Ω, R1, +15 V, 15 V, 0, 330 Ω, 5.1 Ω 5 W, R2, 50 Ω, 100 Ω, 430 Ω, 39 Ω, −5.2, 250 µF All Diodes — 1N4934 All NPN — MJE200 All PNP — MJE210 Adjust R1 to obtain I_{B1} For switching and RBSOA, R2 = 0 For $V_{CEO(sus)}$, R2 = ∞	TURN–ON TIME I_{B1} I_{B1} adjusted to obtain the forced h_{FE} desired TURN–OFF TIME Use inductive switching driver as the input to the resistive test circuit.
CIRCUIT VALUES	L_{coil} = 80 mH, V_{CC} = 10 V R_{coil} = 0.7 Ω	L_{coil} = 180 µH R_{coil} = 0.05 Ω V_{CC} = 20 V V_{clamp} = 250 V R_B adjusted to attain desired I_{B1}	V_{CC} = 250 V R_L = 50 Ω Pulse Width = 10 µs
TEST CIRCUITS	INDUCTIVE TEST CIRCUIT TUT, 1, INPUT, 1N4937 OR EQUIVALENT, R_{coil}, L_{coil}, SEE ABOVE FOR DETAILED CONDITIONS, V_{clamp}, V_{CC}, 2, RS = 0.1 Ω	OUTPUT WAVEFORMS I_C, $I_{C(pk)}$, t_r Clamped, t, t_1, t_f, V_{CE}, V_{CE} or V_{clamp}, TIME, t_2 t_1 Adjusted to Obtain I_C $t_1 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{CC}}$ $t_2 \approx \frac{L_{coil}(I_{C_{pk}})}{V_{Clamp}}$ Test Equipment Scope — Tektronix 475 or Equivalent	RESISTIVE TEST CIRCUIT TUT, 1, 2, R_L, V_{CC}

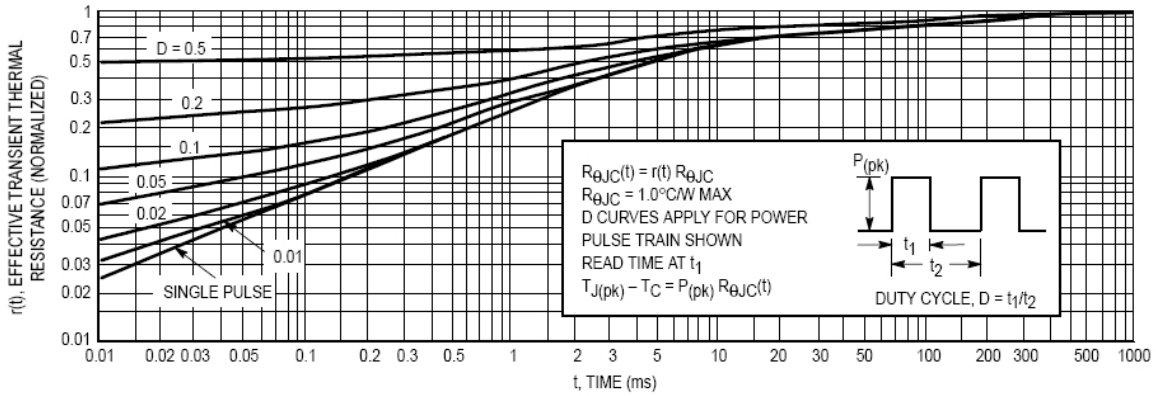

Figure 11. Thermal Response

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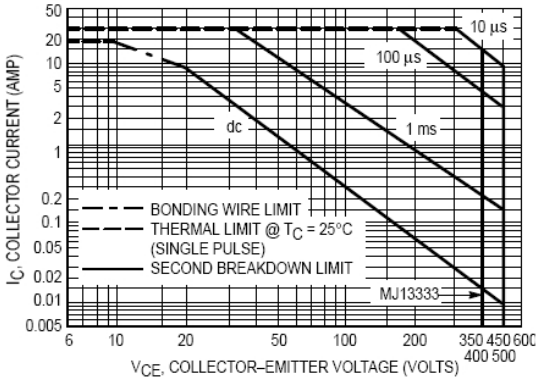

Figure 12. Forward Bias Safe Operating Area

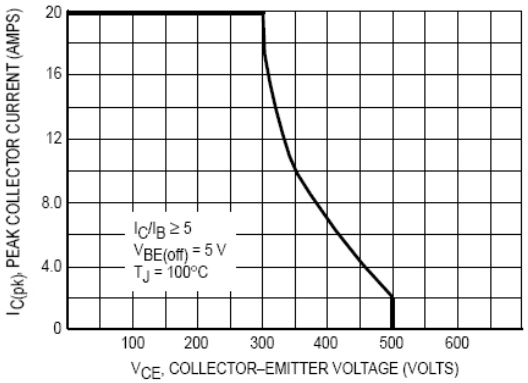

Figure 13. RBSOA, Reverse Bias Switching Safe Operating Area

SAFE OPERATING AREA INFORMATION

FORWARD BIAS

There are two limitations on the power handling ability of a transistor average junction temperature and second breakdown. Safe operating area curves indicate $I_C - V_{CE}$ limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 12 is based on T_C = 25°C. $T_{J(pk)}$ is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when $T_C \geq 25$°C. Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 12 may be found at any case temperature by using the appropriate curve on Figure 14.

$T_{J(pk)}$ may be calculated from the data in Figure 11. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

REVERSE BIAS

For inductive loads, high voltage and high current must be sustained simultaneously during turn–off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage–current condition allowable during reverse biased turn–off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 13 gives the complete RBSOA characteristics.

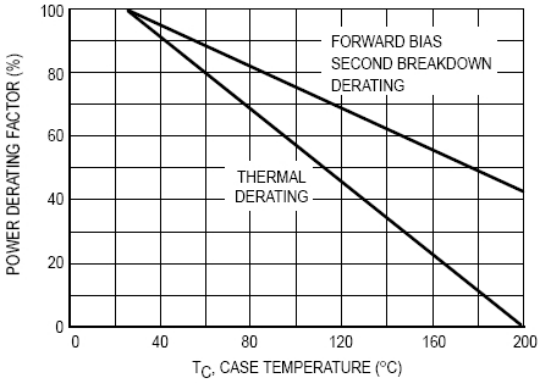

Figure 14. Power Derating